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IC and Component Selection for Space Systems*

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**focus is on active components and not passive*

To be presented by Kenneth LaBel at 9th European Conference Radiation and Its Effects on Components and Systems (RADECS07) Short Course Session, Monday, September 10, 2007 - Deauville, France.

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Outline

- Semiconductors: The Evolution of ICs
  - Availability and Technology
- IC Selection Requirements - three fields of thought
  - Technical – the designer: "The Good"
  - Programmatic – the manager: "The Bad"
  - Risk – the radiation/reliability engineer: "The Ugly"
- Radiation Perspective - Four methods of selecting ICs for space systems
  - Guaranteed hardness
    - Radiation-hardened by process (RHBP)
    - Radiation-hardened by design (RHBD)
  - Historical ground-based radiation data
    - Lot acceptance criteria
  - Historical flight usage
  - Unknown assurance
- Understanding Risk
  - Risk trade space
  - Example: ASICs and FPGA – sample selection criteria
- Conclusions

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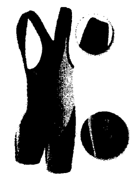
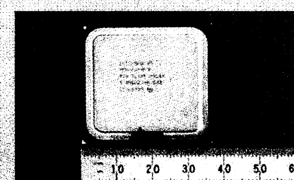
The Growth in IC Availability

- The semiconductor industry has seen an explosion in the types and complexity of devices that are available over the last several decades
  - The commercial market has driven items such as
    - High density (memories)
    - High performance (processors)
    - Upgrade capability and time-to-market (FPGAs)
    - Wireless (RF and mixed signal)
    - Long battery life (Low-power CMOS)



Integrated Cycling Bib and MP3

Zilog Z80 Processor
circa 1978
8-bit processor



Intel 65nm Dual Core Pentium D Processor
circa 2007
Dual 64-bit processors

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The Changes in Device Technology

- Besides increased availability, many changes have taken place in
  - Base technology,
  - Device features, and,
  - Packaging
- The table below highlights a few selected changes

Feature	circa 1990	circa 2007
Base technology	bulk CMOS/NMOS	CMOS with strained Si or SOI
Feature size	> 2.0 um	65 nm
Memory size - volatile (device)	256 kb	1 Gb
Processor speed	64 MHz	> 3 GHz
FPGA Gates	2k	> 1M
Package	DIP or LCC - 40 pins	FCBGA - 1500 balls
Advanced system on a chip (SOC) features	Cache memory	>Gbps Serial Link, Serdes, embedded processors, embedded memory

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The Challenge for Selecting ICs for Space

- The selection of devices has become more daunting in that considerations have changed since the "old days"
  - High reliability (and radiation tolerant) devices
    - Now a *very* small market percentage
  - Commercial "upscreening"
    - Increasing in importance
    - Measures reliability, does not enhance
  - System level performance and risk
    - Hardened "systems" not devices

ADCs? *SerDes?* *SDRAM?* *Processor?* *ASICs?* *DSPs* *FPGAs?* *Flash?*

System Designer – *Trying to meet high-resolution instrument requirements AND long-life*

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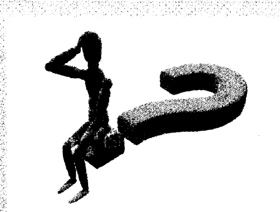
IC Selection Requirements

- To begin the discussion, we shall review IC selection from three distinct and often contrary perspectives
  - Performance,
  - Programmatic, and,
  - Reliability.
- Each of these will be considered in turn, however, one must ponder all aspects as part of the process



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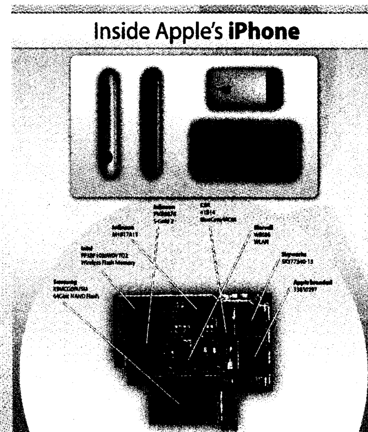
Performance Requirements

- **Rationale**
  - Trying to meet science, surveillance, or other performance requirements
- **Personnel involved**
  - Electrical designer, systems engineer, other engineers
- **Usual method of requirements**
  - Flowdown from science or similar requirements to implementation
    - I.e., ADC resolution or speed, data storage size, etc...
- **Buzzwords**
  - MIPS/watt, Gbytes/cm^3, resolution, MHz/GHz, reprogrammable
- **Limiting technical factors beyond electrical**
  - Size, weight, and power (SWaP)



Performance –
Inside a Apple iPhone™ player

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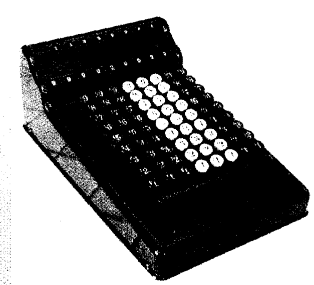
Programmatic Requirements and Considerations

- **Rationale**
  - Trying to keep a program on schedule and under budget
- **Personnel involved**
  - Project manager, resource analyst, system scheduler
- **Usual method of requirements**
  - Flowdown from parent organization/mission goals for budget and schedule
    - I.e., Launch date
- **Buzzwords**
  - Cost cap, GANTT/PERT chart, risk matrix, contingency
- **Limiting factors**
  - Ultimate decision on budget and schedule determined by others



Programmatics –
A numbers game

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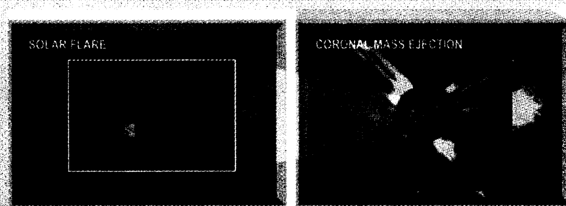
Risk Requirements

- Rationale
  - Trying to ensure mission parameters such as reliability, availability, operate-through, and lifetime are met
- Personnel involved
  - Radiation engineer, reliability engineer, parts engineer
- Usual method of requirements
  - Flowdown from mission requirements for parameter space
    - I.e., SEU rate for system derived from system availability specification
- Buzzwords
  - Lifetime, total dose, single events, device screening, "waivers"
- Limiting factors
  - Usually the final determination of risk acceptance is at a higher management level



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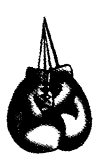
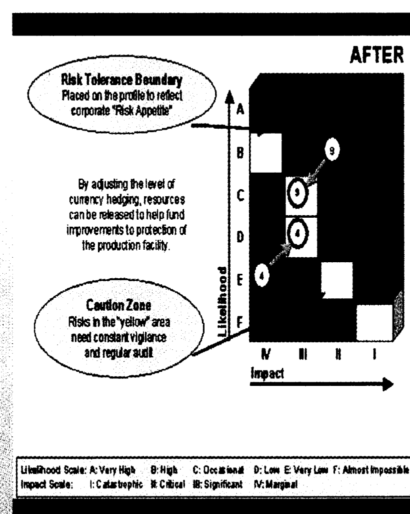
An Example "Ad hoc" Battle

- Mission requirement: High resolution image
  - Flowdown requirement: 14-bit 100 Msps ADC
    - Usually more detailed requirements are used such as ENOB or INL or DNL as well
  - Designer
    - Searches for available radiation hardened ADCs that meet the requirement
    - Searches for commercial alternatives that could be upscreened
  - Manager
    - Trades the cost of buying Mil-Aero part requiring less aftermarket testing than a purely commercial IC
    - Worries over delivery and test schedule of the candidate devices
  - Radiation/Parts Engineer
    - Evaluates existing device data to determine reliability performance and additional test cost and schedule
- The best device? Depends on mission priorities





Traditional Risk Matrix - Corporate

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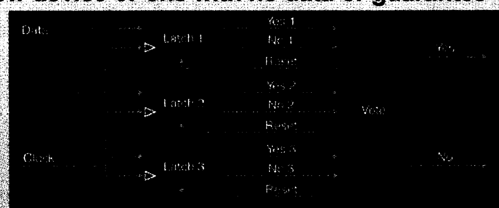
Radiation Perspective on IC Selection

- **From the radiation perspective, ICs can be viewed as one of four categories.**
  - **Guaranteed hardness**
    - **Radiation-hardened by process (RHBP)**
    - **Radiation-hardened by design (RHBD)**
  - **Historical ground-based radiation data**
    - **Lot acceptance criteria**
  - **Historical flight usage**
    - **Statistical significance**
  - **Unknown assurance**
    - **New device or one with no data or guarantee**



RHBD Voting Approach

http://www.aero.org/publications/crosslink/summer2003/08.html

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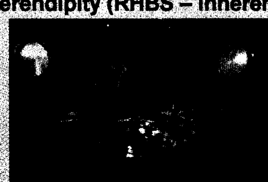
"Guaranteed" Radiation Tolerance

- **A limited number of semiconductor manufacturers, either with fabs or fabless, will guarantee radiation performance of devices**
  - **Examples:**
    - **ATMEL, Honeywell, BAE Systems, Aeroflex**
  - **Radiation qualification usually is performed on either**
    - **Qualification test vehicle,**
    - **Device type or family member, or**
    - **Lot qualification**
  - **Some vendors sell "guaranteed" radiation tolerant devices by "cherry-picking" commercial devices coupled with mitigation approaches external to the die**
- **The devices themselves can be hardened via**
  - **Process or material (RHBP or RHBM),**
  - **Design (RHBD), or**
  - **Serendipity (RHBS – inherent properties of the device/technology)**



Most radiation tolerant foundries use a mix of hardening approaches

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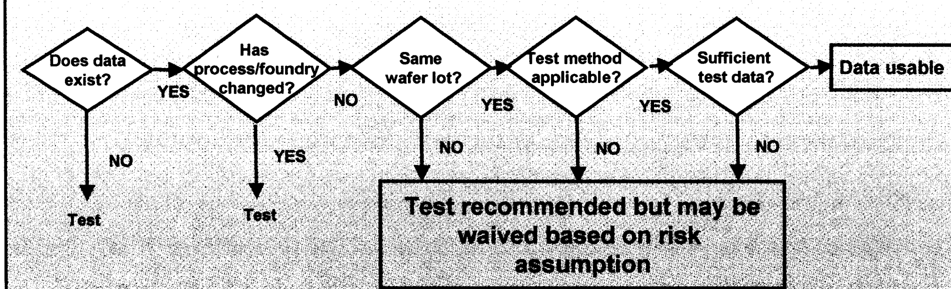
Archival Radiation Performance – Ground-based Data

- **Reviewing existing ground radiation test data and it's application has been discussed previously**
  - **For example. Christian Poivey at NSREC Short Course in 2002**
- **In general, the flow is shown below**



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Archival Radiation Performance – Flight Heritage

- **Many parts have flown in previous space missions**
  - **Can we make use of these parts for new mission?**
- **Similar questions to using archival ground data exist**
  - **Are the parts the same as the "old" ones?**
    - **Lot date codes, process, etc**
  - **Statistical significance of the flight data**
    - **Is the environment it has been exposed to and number of samples sufficient to be statistically of use to the new mission?**
  - **Is the old flight application similar to the new one?**
  - **Has storage of devices affected radiation tolerance?**
  - **And so forth**
- **This approach is rarely recommended by the radiation experts**

Some heritage designs last better than others

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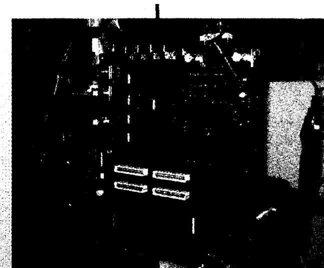
IC's with no Guarantee or Heritage

- ***"Abandon all hope, ye' who enter here"***
  - **Radiation testing is required in the vast majority of cases**
    - **Testing complexities and challenges are discussed elsewhere (e.g., Swift during this short course, LaBel during the conference)**
    - **The true challenge is to gather sufficient data in a cost and schedule effective manner.**
      - **A backup plan should be made in case device fails to pass radiation criteria.**
  - **Exceptions for testing may include**
    - **Operational**
      - **Ex., The device is only powered on once per orbit and the sensitive time window for a single event effect is minimal**
    - **Acceptable data loss**
      - **Ex., System level error rate may be set such that data is gathered 95% of the time. This is data availability. Givien physical device volume and assuming every ion causes an upset, this worst-case rate may be tractable.**
    - **Negligible effect**
      - **Ex., A 2 week mission on a shuttle may have a very low TID requirement. TID testing could be waived.**

FPGA-based motherboard



SDRAM mounted on a daughtercard

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Understanding Risk

- **Risk for a mission falls in to the same topic areas as parts selection**
  - **Technical, programmatic, and reliability**
- **Technical risks**
  - **Relate to the circuit designs not being able to meet mission criteria such as jitter related to a long dwell time of a telescope on an object**
- **Programmatic risks**
  - **Relate to a mission missing a launch window or exceeding a budgetary cost cap which can lead to mission cancellation**
- **Reliability risks**
  - **Relate to mission meeting its lifetime and performance goals without premature failures or unexpected anomalies**
- **Each mission must determine its priorities among the three risk types**

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The Trade Space –

Considerations for Device Selection (Incomplete)

- Cost
  - Procurement
  - NRE
  - Maintenance
  - Qualification and test
- Schedule
- System performance factors
  - Speed
  - Power
  - Volume
  - Weight
  - System function and criticality
  - Other mission constraints (example, reconfigurability)
- System Complexity
  - Secondary ICs (and all their associated challenges)
  - Software, etc...
- Design Environment and Tools
  - Existing infrastructure and heritage
- Simulation tools
- System operating factors
  - Operate-through for single events
  - Survival-through for portions of the natural environment
  - Data operation (example, 95% data coverage)
- Radiation and Reliability
  - SEE rates
  - Lifetime (TID, thermal, reliability,...)
  - "Upscreening"
- System Validation and Verification

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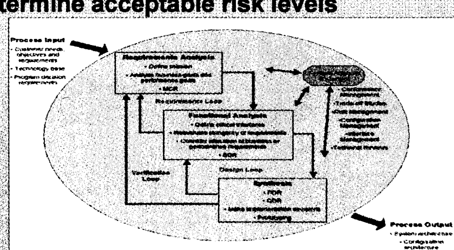
Systems Engineering and Risk

- As is clear from the earlier discussion, the determination of acceptability for device usage is a complex trade space
  - Every engineer will "solve" a problem differently
    - Approaches such as sychnronous design may be the same, but exact implementations are never the same
- A more omnidirectional approach is taken weighing the various risks
  - The systems engineer is often the "person in the middle" evaluating the technical risks and working with management to determine acceptable risk levels



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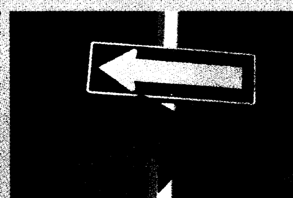
Considerations for Selecting: Custom ASIC (Standard Cell – SC), Structured ASIC (SA), and FPGA

- **Selection criterion will vary for different programs but the following metrics will, in general, be used:**
  - Cost
  - Time to market or program schedule
  - Performance including speed and power
    - Density including embedded circuit options
    - Support circuitry requirements
  - Radiation sensitivity and reliability
- **The following discussion will provide insight into these trades.**



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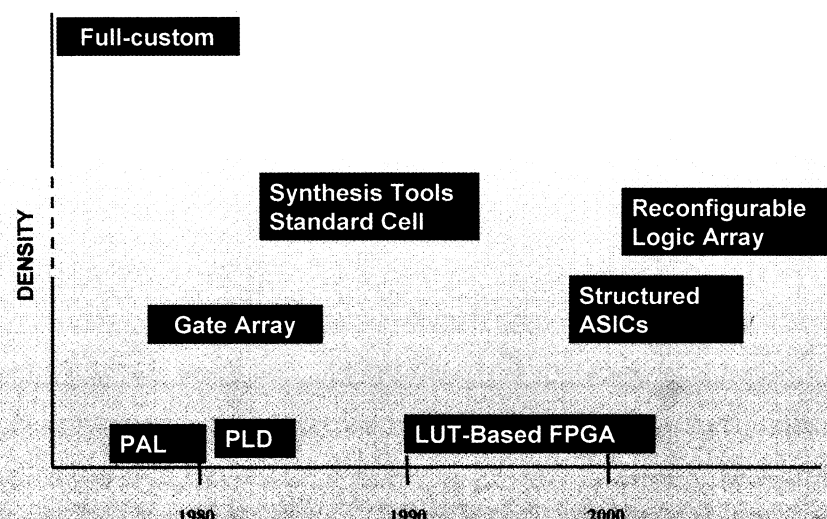
Introduction: Logic Architecture History



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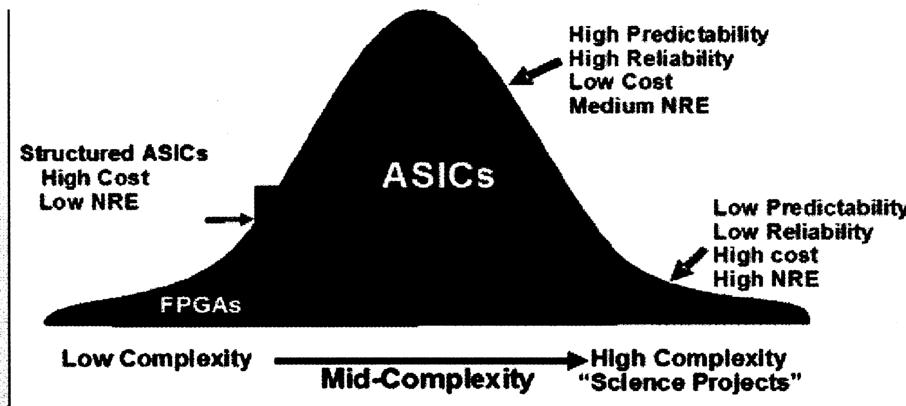
The Trade Space Curve for “Custom” Designs

- Application-specific trade-offs are often made.
  - These trade-offs can impose widely varying requirements



ASICs comprise three separate regions, each with its own complexity, performance and cost characteristics. The position of Structured ASICs on this curve within the mid-complexity region is different for FPGA, traditional ASIC and “design factory” ASIC vendors.

Source: FPGA Journal

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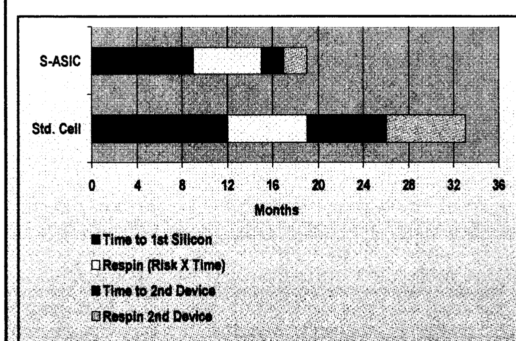
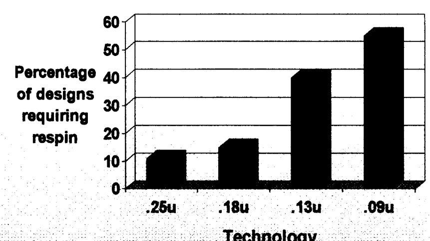
Selection Criteria: Schedule

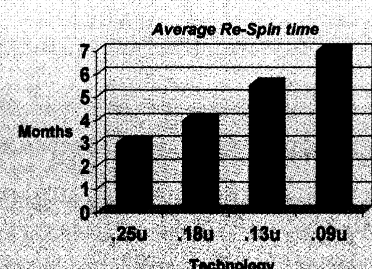
- Time to Market Example
  - 90nm technology
  - < 1Mgate device



FPGA would require ~ ½ the time of the s-ASIC schedule

ASICs and re-spin: a schedule risk





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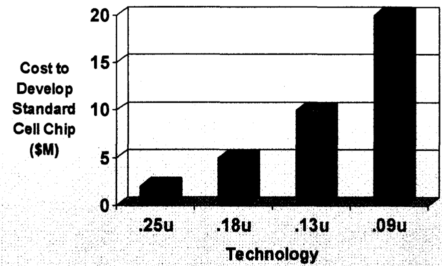
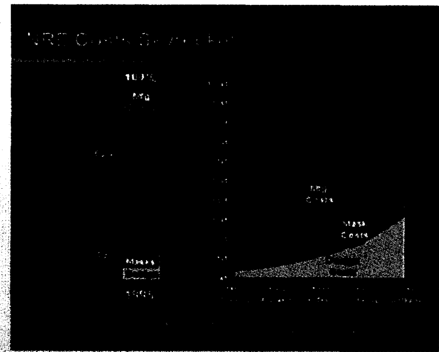
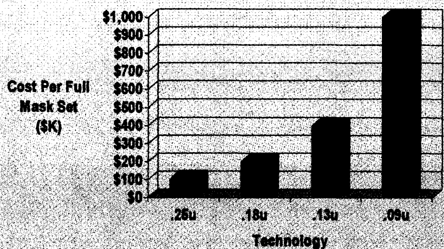
Selection Criteria: Development Cost

- **Standard cell ASIC costs are growing rapidly as feature size has shrunk**







– ***Significant increases in both mask and design costs make strong arguments to support use of SA and/or FPGA approaches wherever possible***

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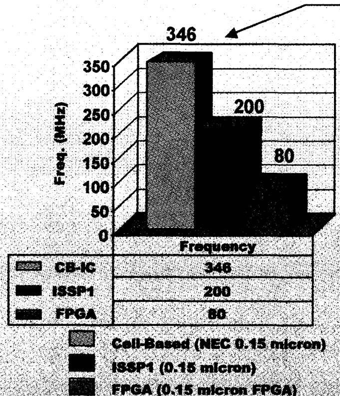
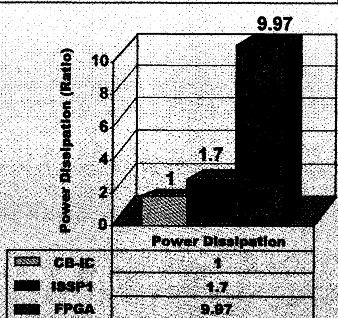
Selection Criteria: Speed and Power

- **Typically, cell based ASIC devices consume less power and can operate at higher speed then either an s-ASIC or FPGA.**
  - **S-ASIC will outperform an FPGA**
    - **However, the performance gap is narrowing with the availability of 65nm FPGA technology manufactured as a power frugal device**

Test Case:
-Telecommunication application module
-- UDL: 300K gates (logic level = 24)





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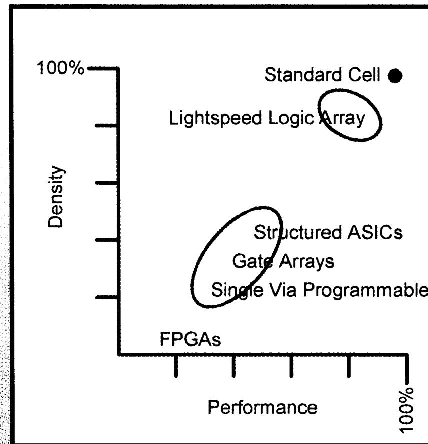
Relative Density and Performance – Best Industry Logic Array

- **Density**
  - **Balanced logic array delivers 80+% the density of standard cell**
- **Performance**
  - **Balanced logic array delivers 80%+ the performance of standard cell**
- **Tuneable**
  - **Can target logic array for performance, density, low power**



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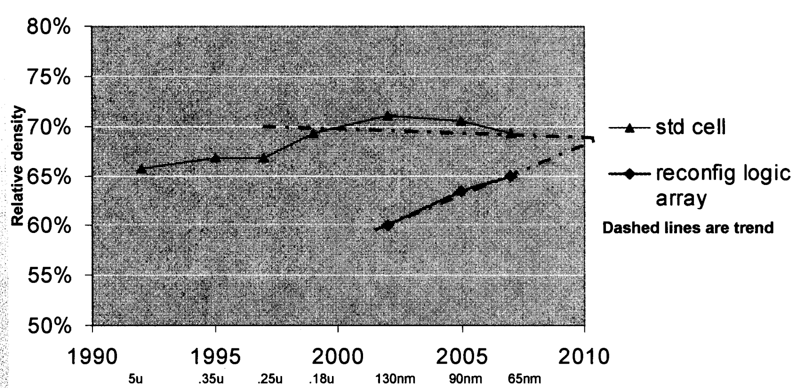
Narrowing Gap between ASICs and FPGAs

– **The data suggests that as technology scales the density difference between custom designs and programmable technologies will converge**

Density vs. Process Theoretical Max



Process Theoretical Max: 2 Input NAND density

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Selection Criteria: Radiation and Reliability

- While there is no "generic" answer for radiation tolerance and reliability levels in the trade, there are numerous considerations such as
  - Is the process radiation tolerant? Was process/device radiation qualification sufficient for planned design or application?
    - Library? Cells? Speed? Etc…
    - Does my performance requirements drive a selection of a specific device type such as reconfigurability or ultra-low power forcing radiation concerns to be worked on the system level?
  - Are radiation results lot-specific (I.e., is lot qualification required)? Application-specific?
  - Does a high-volume commercial foundry provide better or worse reliability than a low-volume high-reliability foundry? Yield? Risk?
  - How does a fault-tolerant system architecture enter the equation?
- As has become more evident, trade spaces are much more complex than "just" an IC

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Radiation Hardening Considerations

- Custom ASIC
  - Unconstrained RHBD and/or RHBP approach to "tune" to required RH level
  - Issues with "Hard" macros and IP in general WRT radiation hardening
  - General issues WRT rad testing and characterization
- Structured ASIC
  - Limited number of RH suppliers
  - Intrinsic TID hardness + SEE RHBD approaches at circuit level, e.g. TMR, scrubbing, and EDAC.
- FPGA
  - Limited number of rad tolerant suppliers, e.g. 100krd
  - Intrinsic TID hardness + SEE RHBD approaches for both configuration control and operational support
    - EDAC, TMR & scrubbing
    - Embedded SEU configuration detection
    - Periodic Configuration read-back
    - Periodic system cycling
    - Dual redundancy

Sample System Complexity for Three Types of FPGA Architectures

OTP | FPGA

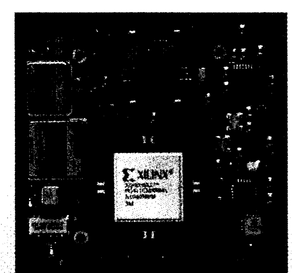
Non-volatile Reprogrammable (Flash) | Circuits to interface between FPGA and ground for new configuration uploads | FPGA

SRAM-based | Circuits to interface between FPGA and ground for new configuration uploads | Watchdog/ controller | FPGA | Non-volatile memory (NVM) – holds configuration of FPGA

Radiation tolerant/hardened options available in all types; Some are "harder" than others

Other Issues

- SRAM Programmable FPGA technology
  - These devices require significant support circuitry including low voltage regulators and SDRAM for configuration storage
  - Support circuitry will require added power and may pose radiation sensitivity problems
    - SDRAM SEE & TID sensitivity
    - LDO ELDRS sensitivity
- Non-volatile Memory Programmable FPGA technology
  - Non-volatile storage element TID and SEGR effects must be considered
- One-time Programmable FPGA technology
  - Reliability issues concerning fuse stability have been identified for at least one manufacturer.
- These constraints and concerns must be carefully assessed in the trade-off process



–Support circuits may limit overall system rad hardness & impose power and reliability constraints

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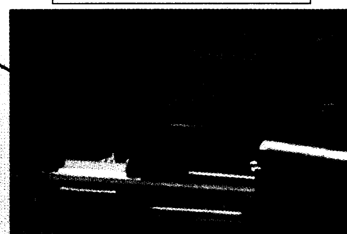
FPGAs –
Related Radiation ad Reliability Concerns

New Silicon
- -90nm CMOS
- -new materials

New Connectors
- -higher-speed, lower noise
- -serial/parallel

New Board Material
- -thermal coefficients
- -material interfaces



New Architectures
- -new interconnects
- -new power distribution
- -new frequencies

New Workmanship
- -inspection, lead free
- -stacking, double-sided
- -signal integrity

New Design Flows/Tools
- -programming algorithms, application
- -design rules, tools, simulation, layout
- -hard/soft IP instantiation

New Package
- -Inspection
- -Lead free

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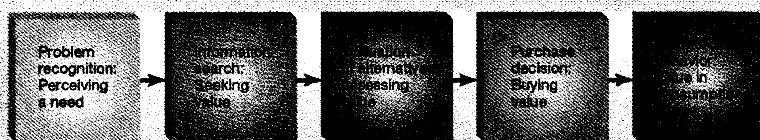
Summary of Generalized Features

Category	SRAM - FPGA	OTP FPGA	S-ASIC	C-ASIC
NRE	Low	Low	Med	High
Production Cost	High	High	Med	High
Risk	Low	Low	Med	High
Development Span (TTM)	Low	Low	Med	High
Electrical Performance	Low	Low	Med	High
Density/Capacity	Low	Low	Med	High
Power Consumption	High	Med	Med	Low
Flexibility	High	Med	Med	Low
Radiation Performance	Low	Med	High	High

Conclusions

- In this talk, we have presented considerations for selection of ICs for space systems
  - Technical, programmatic, and risk-oriented
    - As noted, every mission may view the relative priorities between the considerations differently
- We have also noted a specific type of example, that of custom to semi-custom devices
- As seen below, every decision type may have a process. It's all in developing an appropriate one for your application.



Five stages of Consumer Behavior

http://www-rohan.sdsu.edu/~renglish/370/notes/chapt05/